Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Original) A method for generating an optimized circuit that implements a program implemented in programmable logic, the method comprising:

analyzing a circuit implemented in the programmable logic for possible optimizations; and

optimizing the circuit into the optimized circuit to provide a more efficient implementation of the program by executing a portion of the program using software constructs, wherein using software constructs comprises establishing communications between the programmable logic circuit and at least one software device.

2. (Original) The method of claim 1 wherein analyzing the circuit comprises using a software-to-hardware compiler to analyze the circuit at a later stage in a compilation.

3. (Original) The method of claim 1 wherein analyzing the circuit comprises analyzing the circuit's critical path.

4. (Original) The method of claim 1 wherein optimizing the circuit comprises placing at least one register in the circuit.

5. (Original) The method of claim 1 wherein optimizing the circuit comprises placing at least one FIFO in the circuit.

6. (Original) The method of claim 1 wherein optimizing the circuit comprises placing at least one interface buffer in the circuit.

7-22. (Canceled)

23. (New) A software-to-hardware compiler for optimizing a circuit that implements a program implemented in programmable logic, the compiler configured to:

analyze a circuit implemented in the programmable logic for possible optimizations; and

optimize the circuit into the optimized circuit to provide a more efficient implementation of the program by executing a portion of the program using software constructs, wherein using software constructs comprises establishing communications between the programmable logic circuit and at least one software device.

24. (New) The software-to-hardware compiler of claim 23 further configured to analyze the circuit at a later stage in a compilation.

25. (New) The software-to-hardware compiler of claim 23 further configured to analyze the circuit's critical path.

26. (New) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one register in the circuit.

27. (New) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one FIFO in the circuit.

28. (New) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one interface buffer in the circuit.